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This report covers the first two quarters of the AOSP Memory Program. The Program is focused on the development of a low power GaAs static memory technology capable of 4K bit complexity levels. Work covered during the initial phase of this program includes verification of the low power memory cell design, evaluation of extremely low current GaAs MESFETs and Diodes, process development on M Ω CERMET resistors, design and digitization of a preliminary RAM Test Mask and plans for the 4K bit RAM design.

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FOREWORD

The research covered in this report is carried out in a team effort at Rockwell International Microelectronics Research and Development Center. The program is sponsored by the Defense Sciences Ofice of the Defense Advanced Research Projects Agency. The Rockwell program manager is Fred. H. Eisen. The co-principal investigtors are:

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MICROELECTRONICS RESEARCH AND DEVELOPMENT CENTER

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TECHNICAL SUMMARY

This report covers the first six months of the AOSP GaAs Memory Program. The objective of this program is to utilize the performance advantages offered by GaAs integrated circuits in the areas of radiation hardness, low power dissipation and high speed for the development of a 4K bit RAM. The DARPA process development program has complemented and provided a sound basis for the initial progress made in this RAM program. Using the existing GaAs technology as a base we have initially focused our efforts on process areas unique to RAMS and on evaluation of the proposed power concentration RAM cell apparoach.

Work which took place during the first two quarters of this program concentrated in he areas of MΩ resistor processing, low threshold device characterizastion, RAM circuit design and mask fabrication required for the RAM development program.

MΩ Resistor Development

One of the main process development activities of this program is the development and evaluation of a MΩ resistor process. Extremely high value (up to 200 MΩ) resistors are required for the proposed low power RAM cell. CERMET ($Cr:SiO_x$) films are being evaluated for this application. Various CERMET deposition approaches were evaluated leading to the election of workable RF diode sputtering method. Using this technique CERMET resistor films exhibiting 1-30 MΩ/□ resistivities have been reliably obtained. In addition, a resistor replication technique using ion milling has been successfully

demonstrated during this reporting period. Initial work on the fabrication of CERMET resistors indicates that this is a viable process approach for achieving MΩ resistors. Full evaluation of this resistor approach applied to actual RAM cells will be conducted on the first RAM mask set during the third quarter of this program.

Design Verification and Device Characterization

The basic power concentration cell initially proposed for this RAM program was analyzed further during the initial design phase of this program. As a result of this analysis, except for one slight design change now incorporated in the circuit, a positive conformation of this design has been made. A potential risk was identified which is associated with the low power RAM cell design requiring fabricability of the extremely low current devices. However, initial experimentation and evaluation has verified that both the subthreshold and leakage currents of GaAs FETs and diodes behave in a predictable manner and should be manageable in this extremely low power circuit application. Therefore, all of the basic ideas initially proposed for use in the development of a 4K bit RAM have been found to be workable. Additional work is needed to completely analyze and verify these approaches, however our current knowledge base has been adequate to commit to the design of the first RAM mask set.

RM1 Mask Design

An initial RAM mask set has been designed and digitized in order to test the proposed RAM cell concepts, fabrication processes and design layout

rules. This mask is a vehicle which is meant to provide a fast turnaround on RAM cell design fabrication, test and evaluation prior to committing to a technology approach suitable for the 256 bit RAM. This mask contains a large matrix of RAM circuit designs and RAM cell layouts, descrete FETs and diodes for low current device characterization, CERMET resistor test structures and small RAM cell arrays with and without on chip MΩ resistors. At the end of this reporting period this mask was in-house. A minimum number of wafer lots (3-4) will be fabricated using this test material. Results obtained from these wafers will provide the data for a proven design of a 256 bit RAM in a reasonable time frame. With this approach, results on 256 bit RAMs should be obtained before the end of the 4th quarter.

4K bit RAM Chip Layout

Preliminary RAM cell designs and process development tasks are underway. In parallel to these efforts, the design strategy and layout organization for a 4K bit RAM is also in progress. The 4K bit RAM chip will consist of a 64 × 64 array of special power concentration cells. Similarly in order for the peripheral logic gates to be compatible with the low power budget, it is proposed to design peripherals with automatic powerdown circuitry concepts. A preliminary design and layout of a 4K bit RAM with full peripherals has been achieved.

1.0 INTRODUCTION

The objective of this program is to utilize the performance advantages offered by GaAs integrated circuits in the areas of radiation hardness, low power dissipation and high speed for the development of a 4K bit RAM. Under our DARPA process development program, great strides have been made toward successful development of an ion implanted planar GaAs LSI/VLSI compatible processing technology. This GaAs technology development program has ideally complemented and provided a sound basis for the initial RAM development. The technology development strategy used in this program, therefore, extends the existing GaAs technology base process in areas unique to RAMS, utilizes a power concentration RAM cell approach, and integrates both advanced design and processing concepts into a viable GaAs LSI/VLSI RAM technology.

The thrust of our initial work was directed towards the evaluation and verification of the soundness of our proposed low power RAM cell design concepts and fabrication approaches. Several key areas of concern were identified and dealt with during this reporting period. Initial development demonstrating the feasibility of a MΩ resistor process is described in Section 2.1. Low threshold FET and diode device characterization was carried out in order to evaluate the manageability of balancing inherent device subthreshold and substrate leakage current levels with the extremely low current values of active devices (dictated by the low power RAM circuit design). These issues and the design trade-off considerations are discussed in Section 2.2. The proposed RAM power concentration cell was carefully evaluated

(described in Section 3.1) in preparation for the first RAM cell design. It was decided that an initial fast turnaround mask set was in order which would contain numerous RAM cells, FETs, diodes, and resistor test structures. The motivation and description of this evaluation mask vehicle is described in Section 3.2. Consistent with the ultimate goal of this program, a proposed 4K bit RAM chip organization is presented in Section 3.3.

2.0 RAM PROCESS DEVELOPMENT

The realization of high speed, low power GaAs 4K bit RAM chips requires a demonstrated fabrication technology capable of extremely high process yields. The current Rockwell LSI fabrication technology goals using low power Schottky diode FET logic (SDFL) circuit approaches are consistent with the requirements of this program. The development of a GaAs IC technology that is compatible with this RAM circuit application has been the focus of the DARPA Ion Implantation Planar GaAs IC Processing program.[1] A full discussion of this fabrication technology can be found elsewhere.[2] Because a low power GaAs RAM cell requires extremely high value load resistors, (20-200 MΩ) and very low threshold FETs (~ 0.5 V) additional process development has been required to implement a GaAs RAM technology. The main focus of the RAM process development to date has been in the development and testing of small, high value resistors.

The MΩ resistor fabrication approach has been to develop thin film cermet (Cr-SiO_x) resistors. A considerable amount of work has been reported[3,4,5] on cermet resistors indicating that both acceptable performance and fabricability may be achieved with this approach. Cermet resistors, in particular Cr-SiO_x, appear attractive since they can be sputter deposited, have high resistivity values, exhibit an acceptable temperature coefficient of resistance, and are compatible with our existing process. In addition, the resistivity can be controlled through the use of bias sputtering[3] and/or oxygen poisoning.[4]

The work done during the last two quarters has been with sputter deposited Cr-SiO films. The results to date are discussed in the following sections.

2.1 Development of High Value Cermet Resistors

The most desirable method of deposition for cermet resistors is RF sputtering as opposed to flash evaporation (maintains proper composition by completely evaporating all the material from the component source) or co-evaporation (each material is simultaneously evaporated from separate sources) techniques. Sputtering provides a more reproducible thin film composition since the sputtering target is composed of a pre-selected metal-insulator composition ratio. Also, the thickness step coverage and uniformity control resulting from sputtering should be superior to evaporation techniques.

2.1.1 Sputter Deposition Techniques

The initial work with cermet film deposition was carried out following the guidelines of Ref. 3. The Cr-SiO_x films were deposited on dielectric coated silicon substrates. For the preliminary runs SiO_2 was the dielectric material, while for the later runs in which resistor test patterns were fabricated, plasma deposited silicon nitride (PSN) was used. The depositions were carried out in a conventional r.f. sputtering system using a 15 cm diameter target of 50-50 wt% Cr-SiO_x. The key system parameters used during the initial depositions was an agron pressure of 6×10^{-3} torr, and a target voltage of 2000 V. As reported in Ref. 3, we found resistivity, as measured

by a four point probe, to be a strong function of substrate bias. However, the absolute value of the resistivity at all bias conditions was several orders of magnitude lower than expected. These results are shown in Fig. 2.1-1. Since the specific resistivity is a very strong function of substrate bias, the relationship between sputtering voltage and power density could be very critical, and thus it was concluded that the target diameter of 15 cm instead of 20 cm, as used in the reference work, led to the different results encountered in this work. After several unsuccessful attempts to increase resistivity values above $\approx 1.8 \times 10^3$ Ω/□ by variation in bias voltage, it was decided to carry out depositions under a partial pressure of oxygen and study its effect on resistivity. In the range of 2.0 to 5.0×10^{-5} torr partial pressure of O_2, the sheet resistivity of the deposited films was found to increase dramatically. These results are shown in Fig. 2.1-2 where sheet resistivity is plotted as a function of oxygen partial pressure, and clearly demonstrate that cermet resistors with the proper resistance are fabricatable. The main drawback to this approach is that the resistivity is such a strong function of both bias conditions and O_2 pressure that it was anticipated that wafer-to-wafer process reproducibility will be very difficult to control. Therefore a practical approach, eliminating the need for O_2 poisoning in order to obtain the proper resistor values was sought out.

A better approach (eliminating O_2 in the plasma) was to increase the dielectric-to-metal ratio in the sputtering target allowing the resistivity to be solely controlled by the sputtering bias conditions. A target with 80:20% by weight SiO:Cr was obtained and the previous experiments were repeated. The

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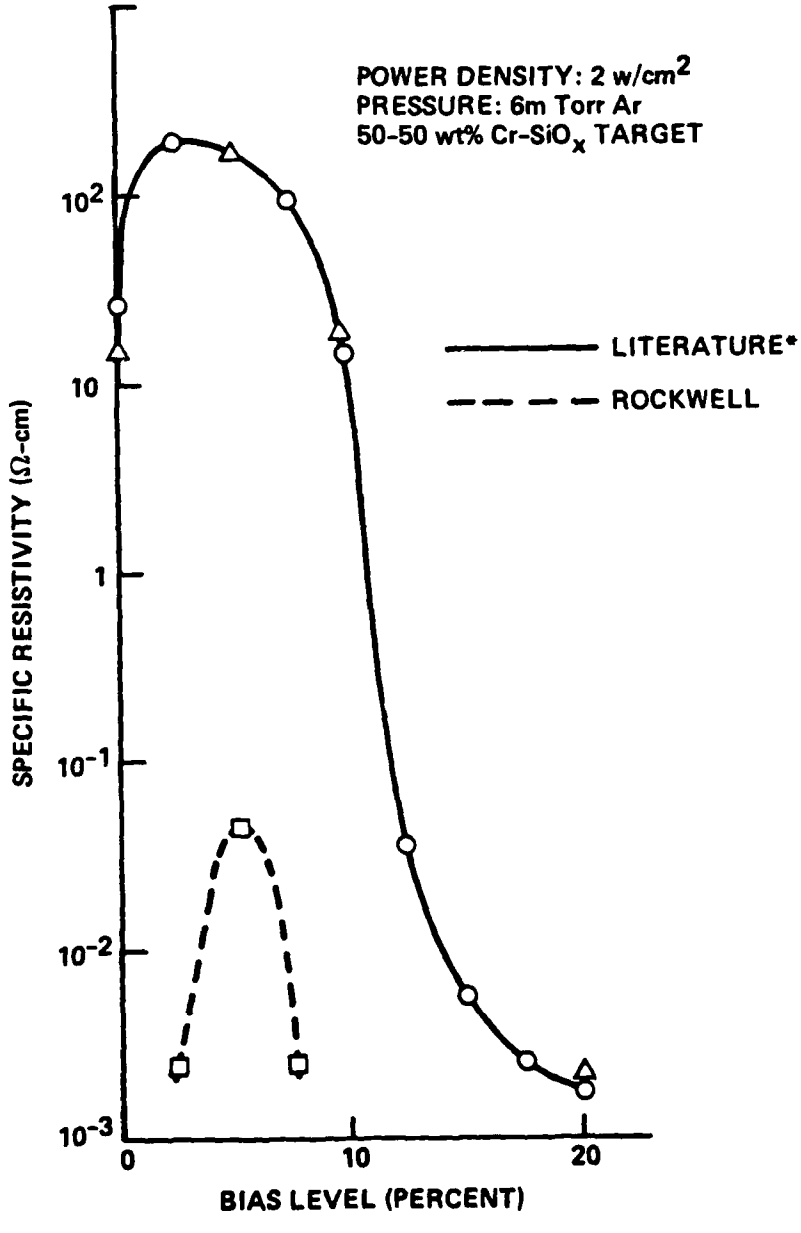

*IBM J. RESEARCH DEVELOPMENT

Fig. 2.1-1 Variation of cermet resistivity with RF sputter bias level

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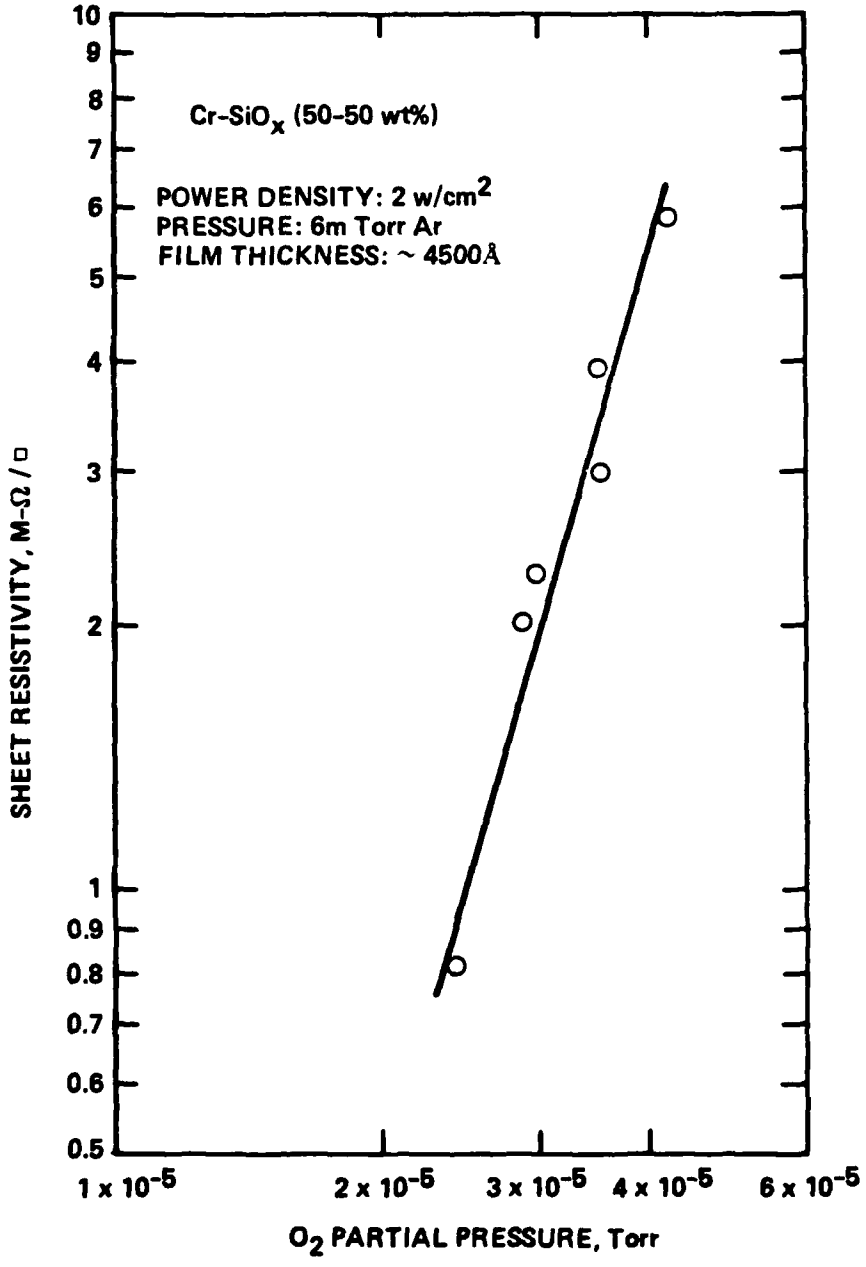
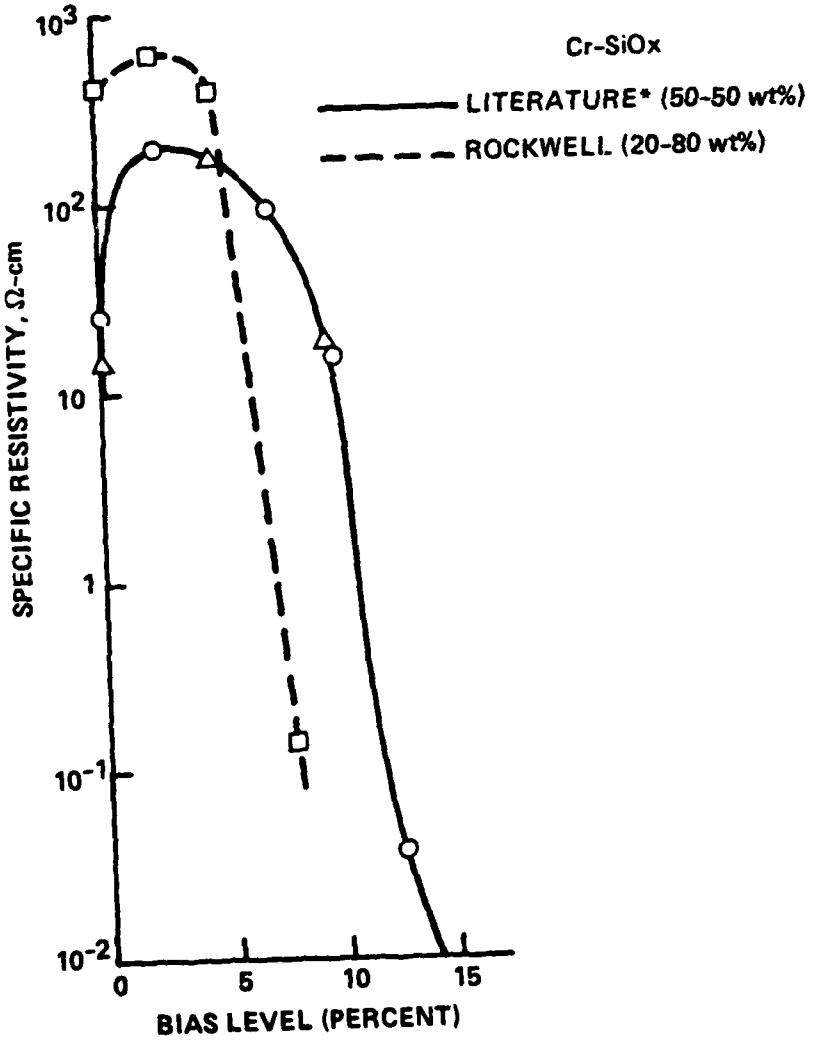


Fig. 2.1-2 Effect of oxygen partial pressure on sputter deposited cermet sheet resistivity.

results are shown in Fig. 2.1-3. A considerable increase in film resistivity was obtained with this target composition with a maximum resistivity value occurring as near a 2.5% bias level. In addition the data in Fig. 2.1-3 shows that using a grounded (non-biased) target results in high resistivity films, demonstrating that cermet films in the range of interest for low power RAM applications can be realized with a simple sputtering technique.

Since it was initially proposed that cermet resistors could be trimmed by ion milling, it was of interest to experiment with the change in resistivity as a function of film thickness. Two films were deposited, one at 0 bias level and the other at 2.5% bias level with an initial thickness of 5600 Å and 6000 Å, respectively. These films were then ion milled for a specific time in order to reduce the film thickness. A new thickness was determined, and the resistivity measured using the four-point probe technique. The results are shown in Fig. 2.1-4. The dashed lines represent the values expected of constant bulk or specific resistivity vs thicknesses calculated from the initial film resistivity and thickness, while the data points are the results obtained from the experimental runs. The films exhibit thickness vs resistiviy in the anticipated manner, indicating that films in the range of 3000 Å should be sufficient for RAM applications.

Since all of the initial runs were carried out at a Ar pressure of ~ 6 mtorr, experiments were now conducted in order to evaluate the effect of pressure on resistivity. The results are shown in Fig. 2.1-5 where sheet resistivity is plotted as a function of the argon pressure during the sputter deposition. The curve is similar to that of the bias voltage effect, and is



*IBM J. RES. DEV.

Fig. 2.1-3 Comparison of cermet resistivity using different sputter target compositions.

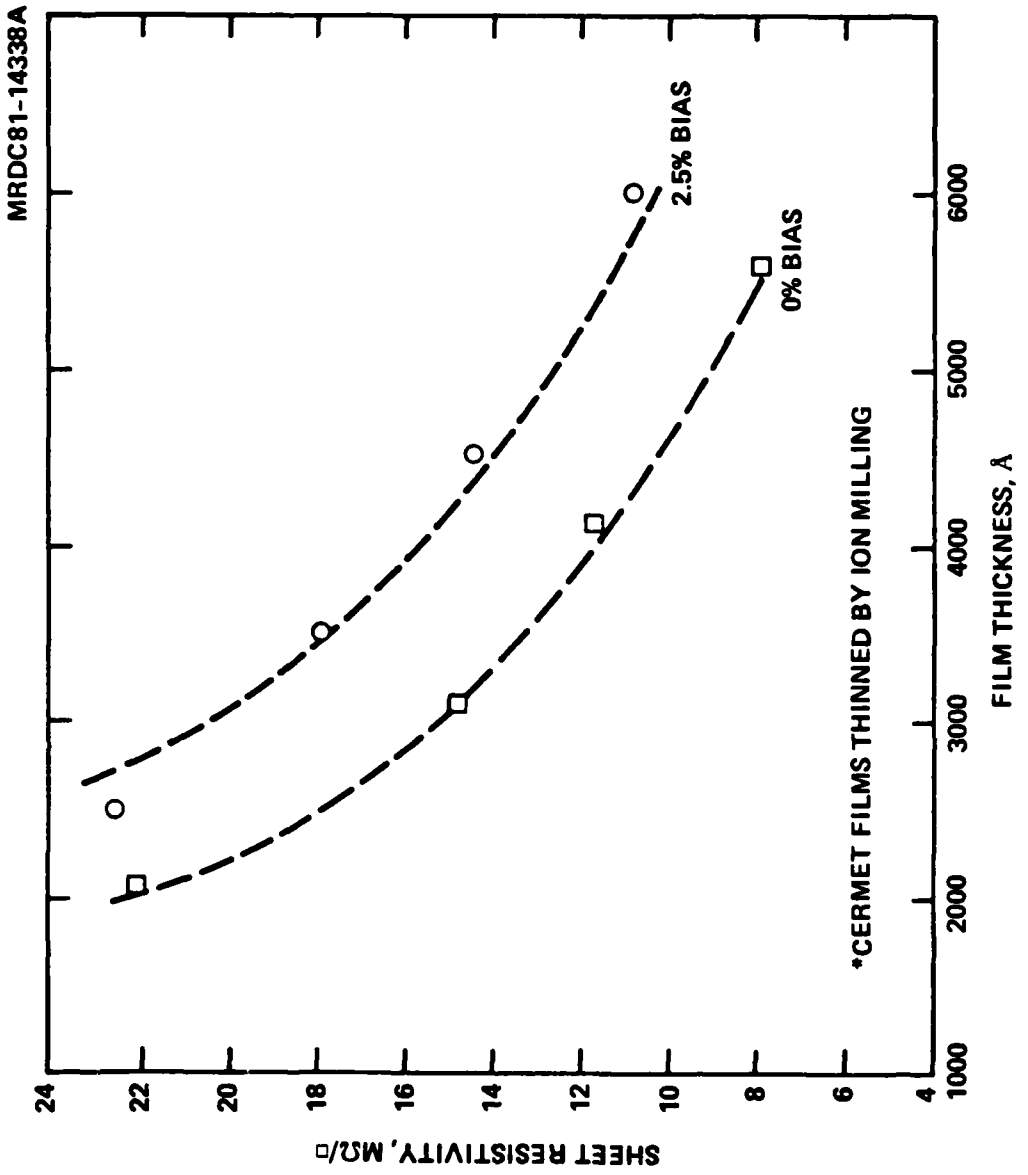


Fig. 2.1-4 Cermet sheet resistivity as a function of film thickness.

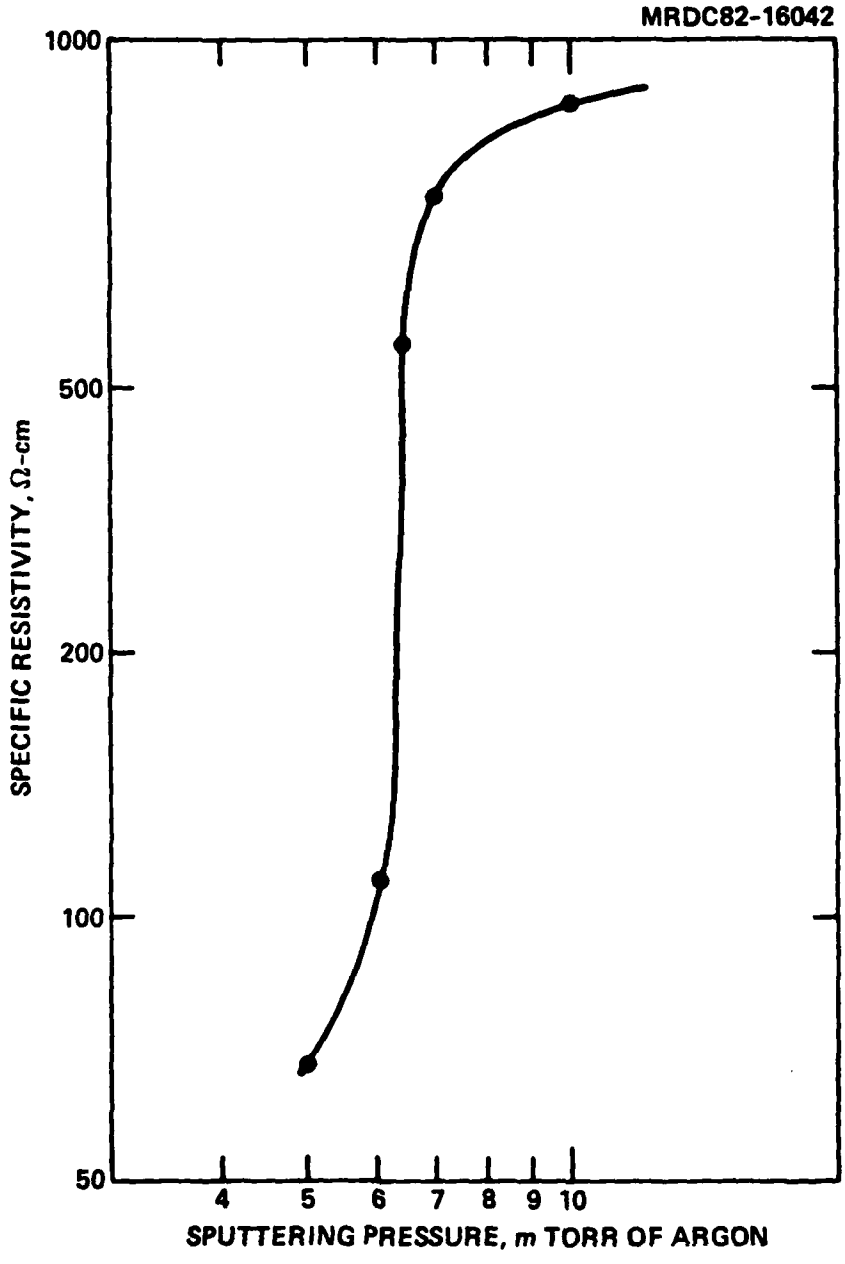


Fig. 2.1-5 Effect of sputtering pressure on cermet film resistivity.

very sensitive in the range of 6-7 mtorr. It is anticipated, therefore, that at the current power level and target composition the sputter depositions will be carried out below 6 mtorr and the desired resistivity will be obtained by choosing the correct film thickness.

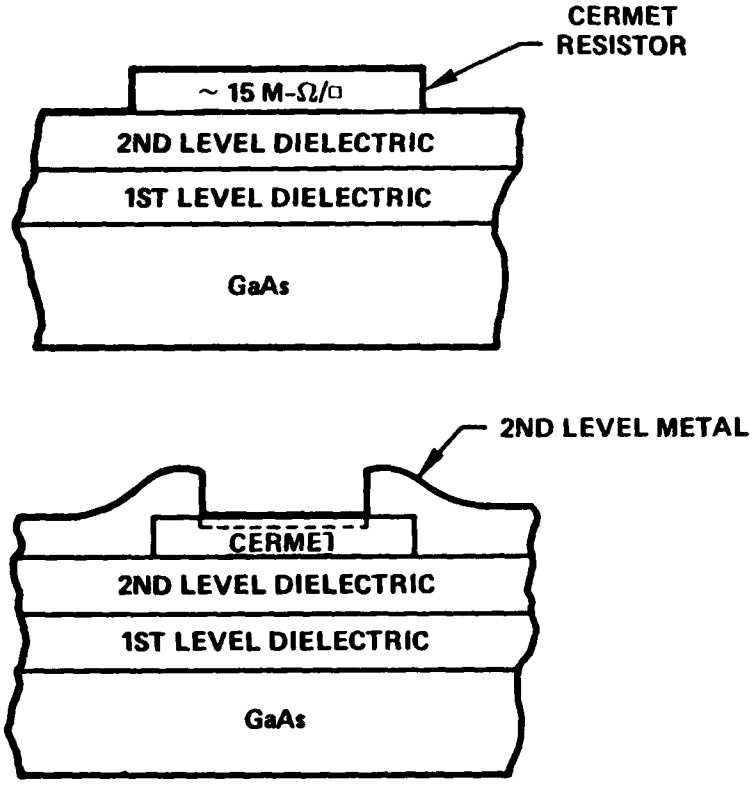
2.1.2 Definition of Resistor Test Patterns

The process which is being pursued for the implementation of cermet thin film resistors for the RAM cell is shown schematically in Fig. 2.1-6. Basically, the appropriate thickness and resistivity of cermet material is deposited on second level dielectric, and the resistors are defined by ion milling. After etching via windows the second level metal is deposited with the interconnects also defined by ion milling. At this point, the resistors can be probed, and adjusted (trimmed) in value if necessary by thinning with additional ion milling. Additional variations to the process will include both thermally stabilizing the cemet resistors and protecting the resistors with a final dielectric layer.

To date, test patterns have been fabricated using only the cermet and second level metal steps. Figure 2.1-7 shows completed resistor test patterns which are then used to determine sheet resistivity and contact resistance.

2.1.3 Measurements and Results

One technique for determining sheet resistivity from the completed resistor test pattern follows the method of Van der Pauw as shown in



FOLLOWING 2ND LEVEL DIELECTRIC:

1. DEPOSIT CERMET FILM
2. MASK CERMET RESISTOR
3. ION MILL RESISTOR
4. MASK VIAS
5. ETCH VIAS
6. DEPOSIT 2ND LEVEL METAL
7. MASK 2ND LEVEL METAL
8. ION MILL 2ND LEVEL METAL
9. SINTER CERMET CONTACT

Fig. 2.1-6 Cermet resister process steps.

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SHEET RESISTIVITY AND
CONTACT RESISTANCE

HIGH VALUE
SERPENTINE RESISTOR

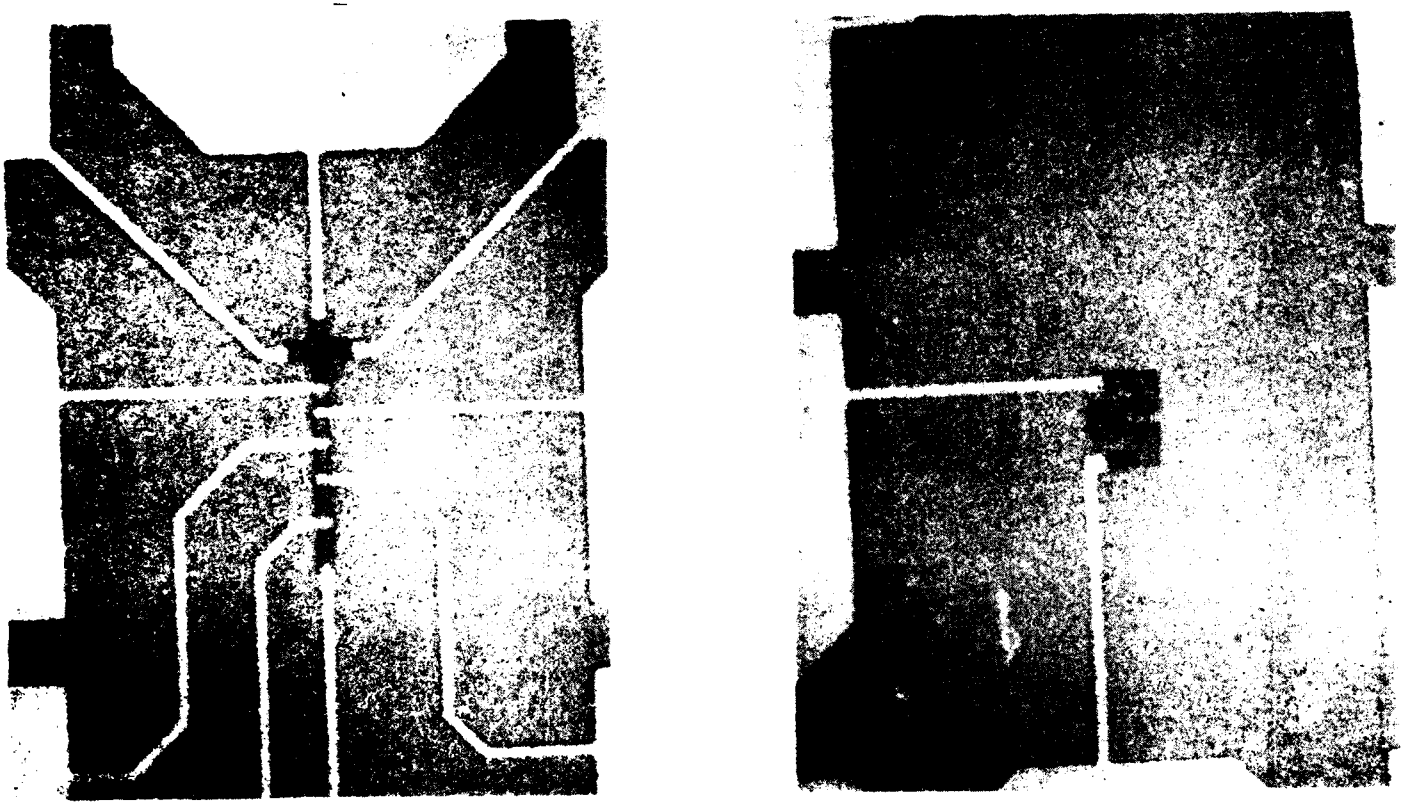


Fig. 2.1-7 Test patterns for cermet resisters.

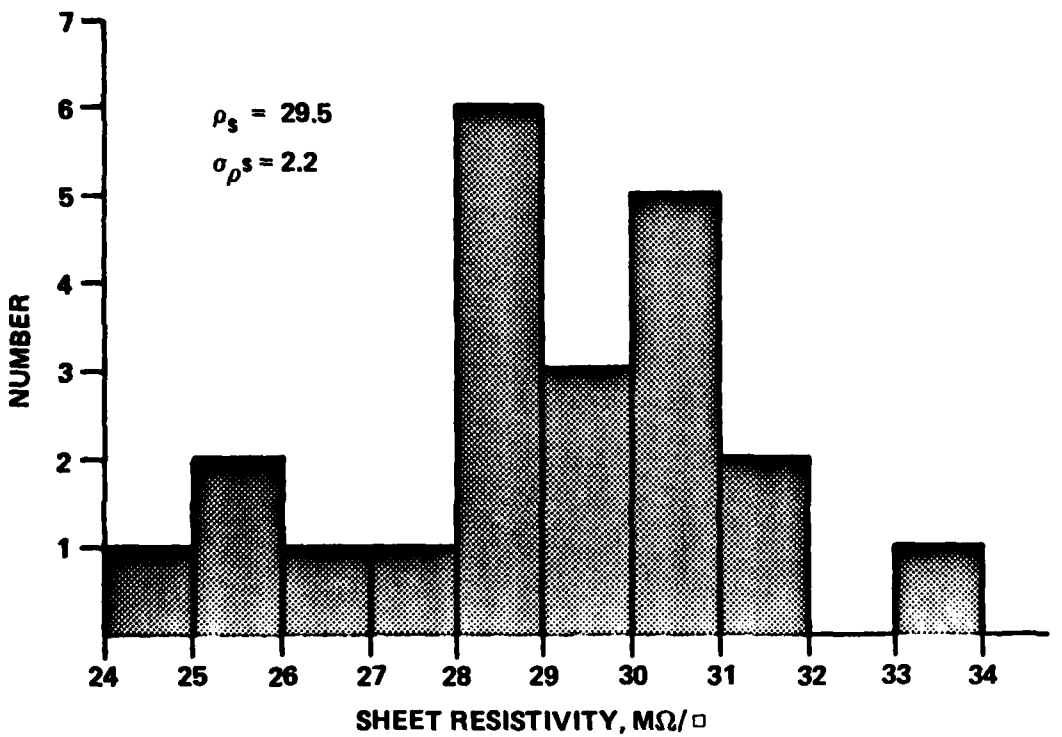
Fig. 2.1-8. Using a current source along with a high impedance voltmeter, a measure of the final resistivity can be obtained. Results for a particular wafer with 4000 A thick, 2 μm wide resistors are also shown in Fig. 2.1-8. The mean resistivity measured by this technique was ≈ 30 MΩ/ .

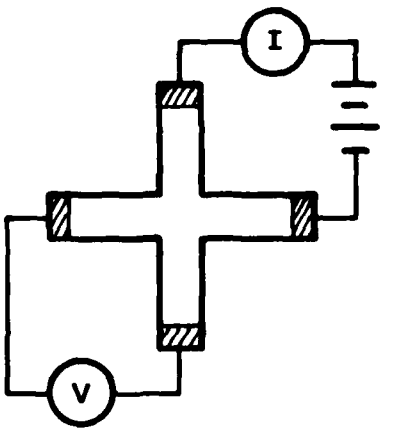
Another more direct method to determine sheet resistivity as well as contact resistance is by the transmission line method (TLM)[6] as shown in Fig. 2.1-9. By using voltage taps along known lengths of resistor, a measure of contact resistance can be determined. The slope of the resistance vs length curve is then used to determine the sheet resistivity. Typically, the TLM indicates a resistivity slightly higher than that of the Van der Pauw technique and is usually in good agreement with the meander resistor also on the test pattern. As shown, a contact resistance of ≈ 5MΩ is typical for a 30 MΩ/□ resistor, and tests are presently being conducted in order to lower this value through contact sintering techniques.

2.1.4 Summary and Plans

During the past reporting period we have fabricated test resistors of Cr-SiO_x with sheet resistivities in the range necessary for proper RAM cell operation (2-30 MΩ/□). The resistivity of the sputter deposited films can be controlled by a number of factors including

target composition,
target bias voltage, and
oxygen poisoning.





4-POINT MEASUREMENT

Fig. 2.1-8 Histogram of cermet resistivity measurements.

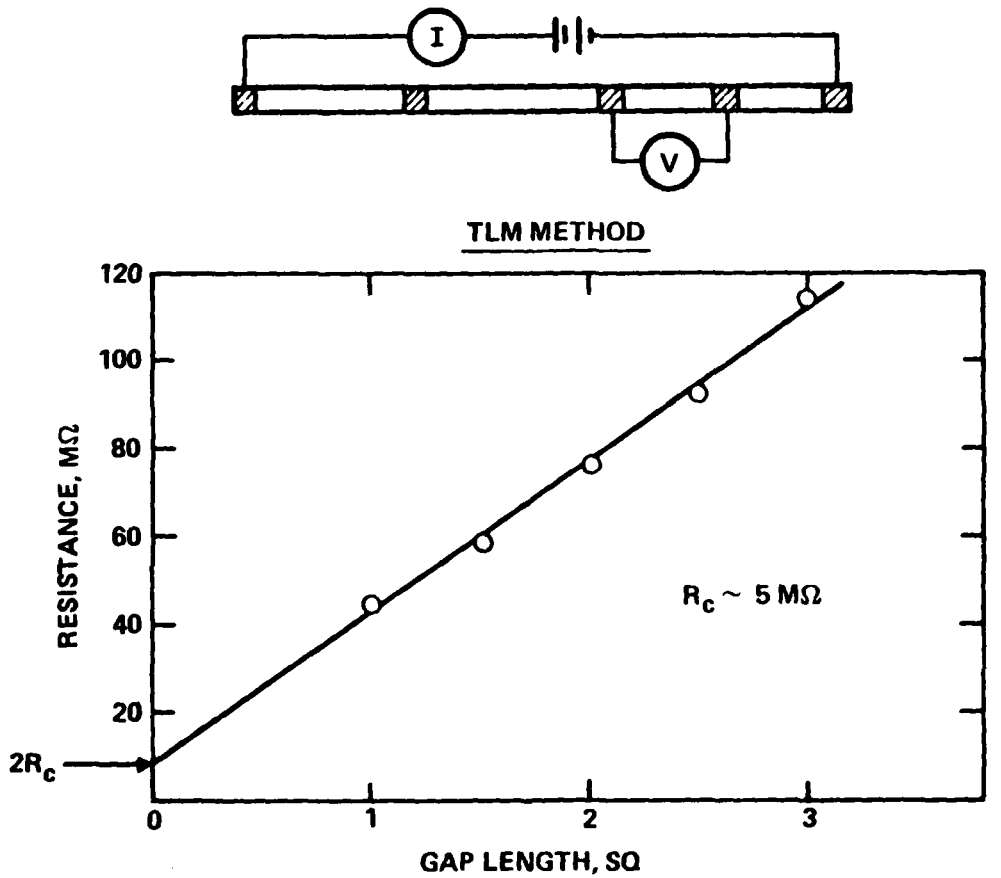


Fig. 2.1-9 Evaluation of cermet contact resistance and sheet resistivity.

The films can be successfully ion milled for pattern delineation which, in turn, is compatable with present fabrication techniques. Redeposition during ion milling and contact resistance are areas which deserve further study.

Work is presently underway to fabricate completed RAM cells with on-chip resistors in an effort to determine over-all fabrication techniques, uniformity, and consistent operation. In addition, consideration is being given to equipment modifications, i.e., planetary fixturing which will help produce more repeatable and uniform depositions of the cermet films. Future cermet design goals will be focused on reproducibly fabricting 8 MΩ/□ resistors with ≤ 1 MΩ/□ contact resistances.

2.2 Subthreshold Currents

To date the majority of expertise developed in high speed GaAs digital IC technology corresponds to circuits operating in rather high current density domains. However, the current levels at which the circuit components will operate in the proposed low power RAM cell are extremely low. For example, logic diodes in a SDFL gate operate at currents on the order of 100 μA, which for a 1 μm × 2 μm area corresponds to a current density of 5000 A/cm^2. In a RAM cell the diodes will be required to operate at a current level between 10 and 100 nA, which corresponds to a current density of 0.5-5 A/cm^2, 3-4 orders of magnitude lower than the current density in the SDFL gate. Even more remarkable is the difference in the currents for the FETs. In an SDFL gate, a FET device with a threshold voltage of -0.75 V will carry a current of ~ 30 μA/μm gate width, and it would be considered "off" at a

current level on the order of 1% of the "on" current, i.e., ~ 0.3 μA/μm. The same FET device in the RAM cell will be considered to be "off" if the current is lower than 10 nA/μm, which is almost two orders of magnitude lower than the off current from the same FET when used in an SDFL gate. The implication of this extremely low current value requirement is that the characteristics of both FETs and diodes, must be re-examined in order to determine whether their low current behavior is acceptable. This means that subthreshold currents and leakage currents must be carefully scrutinized for these devices.

Figure 2.2-1 shows a FET I-V characteristic in the subtheshold current regime. In the figure, the drain current is plotted on a logarithmic scale against gate voltage for a fixed drain voltage of 2.5 V. If this were an ideal device, the current would drop quadratically to zero at the threshold voltage (shown by the dotted line in Fig. 2.2-1). However, the actual device shows an exponential characteristic below threshold, represented by an almost straight line in the figure.

The exponential behavior of the subthreshold current can be easily understood by thinking of the FET channel biased below threshold as a potential barrier between the source and the drain. As the gate voltage is made more negative the height of this barrier increases, and the current decreases proportional to an exponential function of the barrier height, that is the gate voltage (below threshold).

The current corresponding to the "off" state is at the level indicated by a solid horizontal line in Fig. 2.2-1 (after scaling for FET

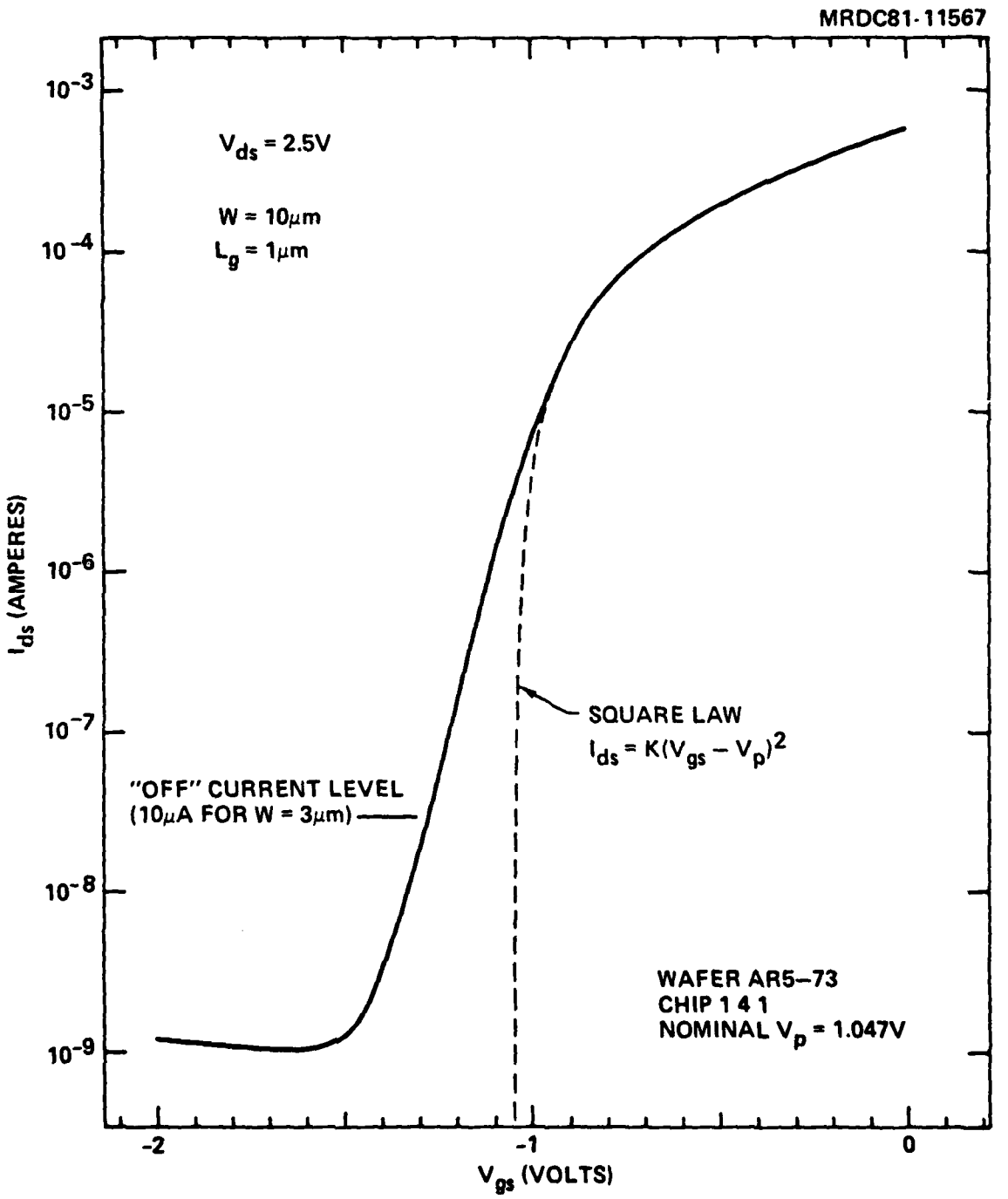


Fig. 2.2-1 Subthreshold portion of the I_{ds} vs V_{gs} characteristic (at V_{ds} = 2.5 V) for a 10 μm wide, 1 μm long gate FET.

width). In order to bring the current down to this level, the gate voltage must be ~ 0.2 V below the nominal threshold voltage. This is quite acceptable value, obtainable with the circuit approach described in Section 3.1.

Although the data on subthreshold current in Fig. 2.2-1 appears promising, several points of caution must be taken into account. First, the data were obtained from a 10 μm wide device. Since the proposed design calls for 2 or 3 μm wide transistors, it will be necessary to verify whether narrower devices behave similiarly well as the wider devices (that is whether subthreshold currents scale with width as one would expect). Second, the type of data shown from one wafer and was only verified on a few single devices over a few wafers. A wider survey should be conducted in order to verify these results. Third, in Fig. 2.2-1 the subthreshold current region is followed (for more negative voltages) by a region where the current becomes constant at a level about 1 order of magnitude below the memory cell "off" current. This constant current background level is attributed to leakage. As long as current leakage remains well below (1 order of magnitude or more) the "off" current level shown in Fig. 2.1-1, it will cause no harm. However, extensive testing will be required to determine whether this is indeed the case. Furthermore, it will also be necessary to determine how this leakage current scales with device dimensions. As explained in Section 3.3, test devices on the RAM cell evaluation mask will provide the necessary information on subthreshold currents and leakage currents.

Figure 2.2-2 shows the IV characteristic of a 2 × 1 μm logic diode from an SDFL gate. This diode is identical to the diode chosen to produce

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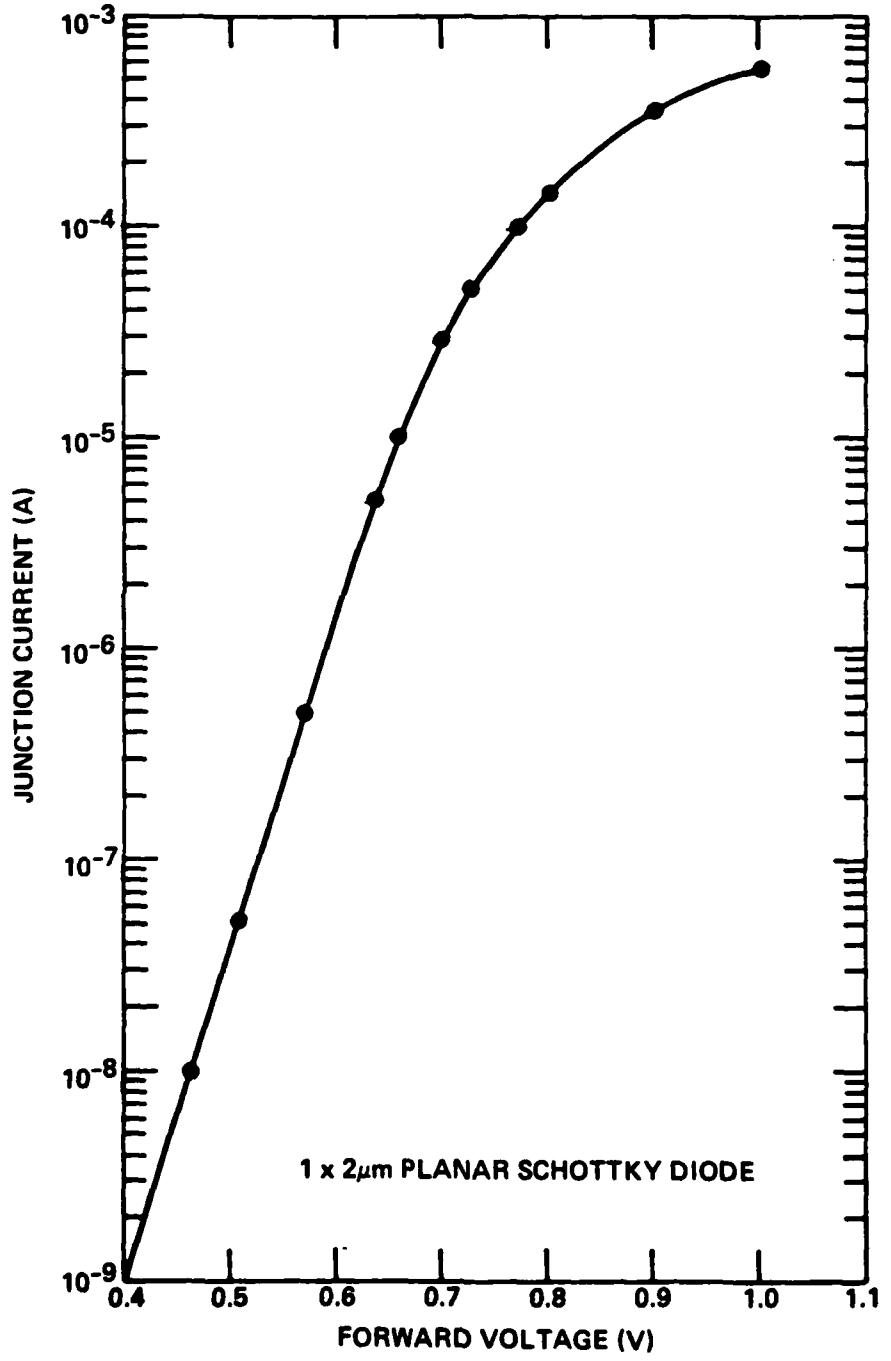


Fig. 2.2-2 I-V characteristic at a 1 × 2 μm area logic diode, to be used in the low power RAM cell.

level shifting in the memory cells. The characteristic in Fig. 2.2-2 is well behaved, exponential as shown by the straight line on a logarithmic plot. The ideality factor is ~ 1.1. The curved portion of the characteristic is due to the series resistance of the diode. This series resistance has no static effect on the RAM cell since the devices operate in a very low current domain. The typical operating current is about 20 nA.

Although the excellent I-V diode characteristic shown in Fig. 2.2-2 indicates that the low current operation of the diode should pose no problem, further characterization of diodes is in order to verify that leakage currents will not occur in the operating current range of the diode.

Figure 2.2-2 also points out that the voltage drop caused by a diode operating in forward bias in the RAM cell will be on the order of ~ 0.45 V, much lower than the typical 0.7-0.8 V which is observed in the SDFL gates where the diodes operate at much higher current densities.

In conclusion, the preliminary data taken from FETs in the subthreshold current regime, and logic diodes at low current levels indicate that the devices are behaving according to predictions, and are well managable for RAM application. However, more extensive testing will have to be carried out to further extend the data base, and to make sure that leakage currents will not interfere with the expected performance.

3.0 CIRCUIT DESIGN

The requirements for memory size and power dissipation are extremely demanding for the AOSP processor array computing elements (ACE). Approximately 2M bits of bulk storage is needed for each of about 20 ACE nodes, and a 100 watt power budget goal has been assigned for the complete AOSP. Allowing for 40% of the power budget in memory, the static power dissipation per bit is only 1 μW. Because relatively few of the 10^4 memory chips (10-100) are actually addressed in a 15 ns system clock cycle, the standby static power dissipation of the memory chip is of far greater significance in reducing total system power then is the chip dynamic power dissipation. Thus, the emphasis in selecting a device and circuit approach for the RAM cell must minimize the static power without undue regard for reducing logic swing (ΔV_o) to reduce dynamic switching energy ($P_D \tau_d$). This static power requirement can best be provided by the depletion-mode MESFET approach described in Section 3.1.

In addition, with a system clock cycle of ~ 10 ns, a relatively high speed circuit design is required while maintaining the low static power. While CMOS would be the natural choice here, MOS silicon approaches are undesirable for this application due to the limited total dose hardness of MOS. Since an equivalent complementary logic technology is not available for GaAs, an approach using only n-channel GaAs MESFETs is required. With this approach, extremely low standby currents and modest but still considerable access speeds must be achieved. These requirements which seem in conflict

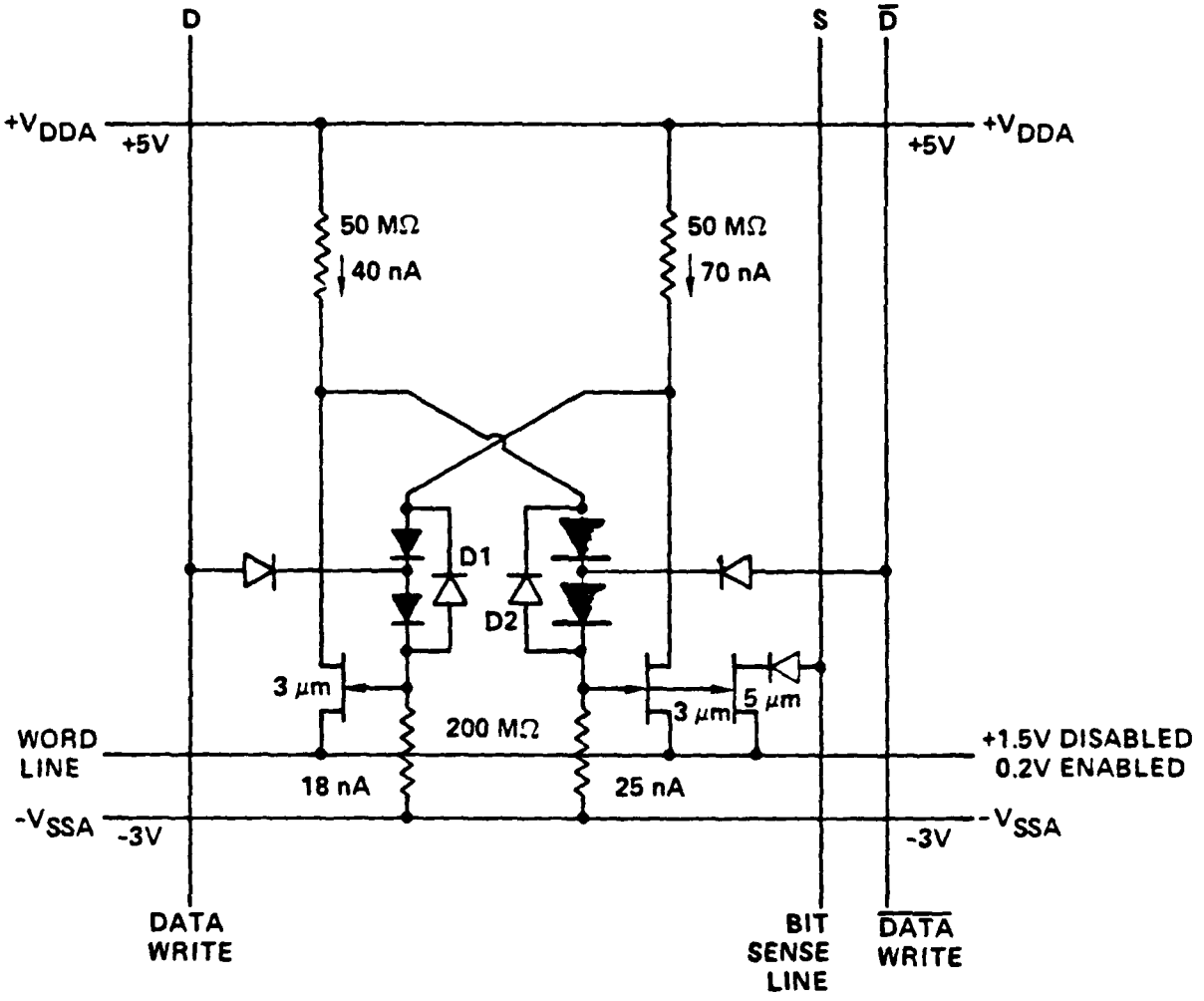
with one another are effectively resolved by the power concentration approach described in Section 3.1.

3.1 Power Concentration RAM Cell

The key design problem for a very low power, moderate access time, 4K GaAs static RAM is not so much the attainment of the T_{acc} ~ 10 ns speed, but obtaining the high speed operation while simultaneously holding the power levels low. Consider, for example, a 4096 cell memory array, arranged 64 x 64. The total bit sense line capacitance on one of these 64 cell columns will be of the order of 425 fF (including overcrossings, line stray capacitance and assuming ~ 2 fF diode capacitance at each cell). For a maximum discharge or charge time of ~ 3 ns, the memory cell would be required to sink a current of 100 μA to achieve a 0.75 V discharge of the sense line capacitance. Clearly, if all 4096 cells operated at 100 μA quiescent current levels, at V_{DD} = 3 V, the static power dissipation would be unacceptably high. Therefore, it becomes mandatory to realize sufficiently fast access time without increasing chip power dissipation.

The solution to achieving adequate readout speeds from the RAM cells without increasing their static power dissipation levels is illustrated in the cell schematic shown in Fig. 3.1-1. The idea is to concentrate power only on the bit cell being accessed, and only while that cell is being read so that the cell, at that moment, has sufficient power available to charge the bit line. This is achieved by making the RAM cell itself capable of operating at much higher current levels in readout than its static operating current

MRDC 80-8122



POWER/BIT = (+5)(110 nA) + (-3)(-43 nA) = 676 nanowatts/bit
MEMORY ARRAY STATIC POWER = 4096 x 676 x 10^{-9} = 2.76 mW/4K CHIP

Fig. 3.1-1 Circuit diagram for the 1 μW RAM cell. Currents shown are for a stored "zero" (left FET "off"), word line deselected (+1.5 V).

levels, and then using the column address demultiplexer to make available relatively high (~ 100 μA) current levels to the cell during bit readout in that column. In the cell example of Fig. 3.1-1, the bit sense line (S), instead of being connected directly to the latch (3 μm FETs with 50 MΩ pull-up resistors), is connected through a diode to the drain of a larger (W = 5 μm) FET, the source and gate of which are in parallel with the 3 μm FET on one side of the latch. This 5 μm FET will be "on" only when a "zero" is stored in the latch. Ordinarily, however, this FET draws no current since either the column is not being accessed (so that no current is supplied to the sense line, S, by the column demultiplexer), or if the column is being accessed, but not this particular row, a + 1.5 V word line voltage at the source of de-selected rows will prevent the diode between the drain of the 5 μm FET and the sense line from conducting. However, if both the column and row are selected, then the word line voltage at the source of this 5 μm output FET will drop to ~ 0.2 V, and the voltage on this bit sense line will be determined by whether or not this particular 5 μm output FET is "on" or "off". The bit sense voltage will be approximately 1 V if a "zero" is stored in the latch and greater than +2 V if a "1" is stored. The current available from a W = 5 μm, V_p = -0.7 V output FET at V_{gs} = +0.5 V would be I_{ds} = 0.4 mA, capable of achieving a voltage slew rate on a C_L = 425fF load of dV/dt = 10^9 V/s, or requiring 600 ps to discharge the bit line by 0.6 V. This should more than adequate for a 10 ns access time RAM.

Operation of this D-MESFET memory cell at this power level requires that the FET subthreshold currents be of the order of 10 nA. This appears

reasonable (see Section 2.2) as long as the logic swing is sufficient to get the gate voltage ~ 0.4 V below "the nominal" square-law threshold voltage (V_p). The large logic swings available in this D-MESFET approach make that possible.

This resistor load RAM cell approach is quite convenient from a technology development standpoint. While the D-MESFETs in the latch operate with only < 100 nA drain currents, they are in fact capable of handling tens to hundreds of microamperes. This means that at earlier development stages, different thicknesses or compositions of the resistor film material may be used to vary sheet resistivity with the same mask to investigate the dependence of yield, radiation tolerance, operating temperature range, etc. on the current level (or static power level) in the cells.

The use of resistor loads in static RAM cells is not a new concept. MOSTEK and other companies have used undoped polysilicon load resistors (~ 50 MΩ) in their commercial NMOS static RAMs for several years. The addition of the high sheet resistivity (~ 10 MΩ/□) resistor layer to the GaAs IC process will require additional development, but appears to be a viable approach because of the highly planar nature of the circuits. The resistor layer will be on top of the second insulator layer and be handled in much the same way that the existing second layer metallization is processed (see Section 2.1 for more details on cermet fabrication).

3.2 RAM Cell Circuit Concept Study

During the first reporting period, the circuit to be used for the 1 μW static RAM cell was analyzed to determine those aspects of the circuit design that required experimental determination or verification. A mask set for fabricating appropriate test circuits and devices was laid out, and digitized on the in-house CALMA system. The aspects of this circuit technology that require experimental evaluation include the characteristics of extremely low current devices, design layout rules, and MΩ resistor characteristics. It is necessary that these factors are characterized and understood accurately to permit an optimum cell to be designed. The importance of optimizing the cell design early in this program cannot be overemphasized. For, while the power concentration circuit approach described in Section 3.1 is a promising method for obtaining both low power and, moderately fast access times on the same chip, the detailed cell design, layout and device characteristics determine the actual power and bit density that can be achieved. It should also be noted that achieving both low power and high bit density has the implicit corollary of an extremely high process.

The first design consideration for the RAM cell, which is basically a latch circuit, is the basic size of the FETs to be used. Large FET widths (≈ 5 μm) have the advantage of being reasonably simple to fabricate with high parametric uniformity. They have the disadvantage of larger cell size and, if the total current in the latch is being established by the requirement for less than 1 μW/cell, very low I_{ds}/I_{dss} ratios. Smaller FETs (down to 1 μm gate width) result in decreased cell size and operate at a more favorable

current density. However, their narrow widths (down to 1 μm) approach the feature size limitations of state-of-the-art processing, which may result in unacceptable yield and large parameter variations from device to device. The operating characteristics of the FETs, and the diodes, are not well known at the low current levels involved, particularly in a densely packed chip where substrate leakage may be of significance. Therefore, both operating characteristics and device yield need to be determined experimentally for a variety of device sizes.

The second design consideration, the layout design rules, have an even greater effect on cell size, and hence bit density, than FET size. These rules are directly derived from the processing steps, and are directly tied to the resolution and layer to layer registration of the photolithographic sequence involved in fabricating the circuits. In this program, it is intended to use the tightest rules that do not degrade yield unacceptably. Yield vs design rule sizes will be determined experimentally. This determination will involve the pattern to be used in the circuit, (i.e., the circuit layout itself) rather than a standardized pattern, so that any proximity or shape dependent effects are automatically taken into account.

Another effect becomes important for closely spaced devices: interdevice leakage currents. These currents are generally not of concern for ordinary logic circuits operating at moderate power levels (0.2-2.0 mW/gate) but increase in importance when interdevice spacing decreases and extremely low operating currents are used. In the proposed RAM cell the leakage currents may be greater than FET "off" currents, and could even become comparable

to FET "on" currents at very high circuit densities. Evaluation of these leakage currents are crucial to a well designed low power RAM.

As indicated in Section 2.1, a final design value for the sheet resistivity of the cermet resistor material to be used in making the MΩ resistors has not been established. Further experimental work is necessary, using test structures specifically designed for the cermet process. This work will involve varying both the resistor sheet resistivity values and aspect ratios. RAM cells will be evaluated using different resistor design trade-offs in order to optimize the circuit performance at the extremely low power levels required.

The resistors in the RAM cell circuit serve to limit the current. The way in which the resistors are fabricated offers the additional benefit of keeping power supply connections on top of the dielectric and off the substrate, thus minimizing substrate effects that can degrade circuit performance. However, the development of a resistor technology with stable, predictable and very high sheet resistivity is not without technical risk, albeit minor, and alternative current limiting means should be evaluated. Potential candidates are reverse biased Schottky diodes, extremely small FETs, or degeneratively connected circuit consisting of a FET and Schottky barrier diodes that self biases near pinchoff. Clearly, design, fabrication and testing of actual devices of the above three types is necessary to determine their applicability to RAM cell design.

These RAM cell experimental evaluation tasks essentially define a mask set. Array sizes must be large enough such each cell tested has an environment of neighboring devices with a layout and density similiar to the projected 4K RAM design. Connections must be direct, so that a maximum amount of information can be derived about the cell and its operation; in a decoded or buffered circuit, very little information can be gathered on individual cell designs, particularly non-functional ones. With the data that can be obtained from a properly designed evaluation mask set, the design of a 256 bit RAM can be accomplished with a high degree of confidence.

Prior to the layout of the first RAM cell mask set, the circuit design was analyzed through a full operating cycle, and all device operating conditions and levels were considered in detail to identify potential problem areas. One problem was found in the circuit. The two diodes in each feedback path (see Fig. 3.1-1) have contradictory requirements. They are used, statistically, to establish a voltage below threshold at the gate of one of the FETs, and, dynamically, to discharge the FET gate capacitance to the write lines. The former requirement is for high current density, and since currents are fixed, small area diodes must be used; the latter requirement is for large capacitance, which implies large area diodes. To overcome this conflict, a reverse biased diode, acting as capacitor, will be added in parallel with the two diodes (D1 and D2 in Fig. 3.1-1). The two forward biased diodes can then be made small, and the reverse biased diode can be made as large as necessary to have a capacitance much larger than the FET gate capacitance.

The evaluation mask set has nine areas, as shown in Fig. 3.2-1; these areas include test vehicles for evaluating all of the design and process technology considerations discussed above.

RAM A and RAM B are 4 × 8 arrays of different RAM cell designs. Each RAM cell is a latch with a sense transistor; the ratio of the latch to sense FET is 1 to 2. RAM A has a variety of cells with 1 and 2 μm FETs, and with 2 and 4 μm FETs; RAM B has the same variety, but with 3 and 6 μm FETs and with 5 and 10 μm FETs. The variety includes designs using resistors with short and long aspect ratios, so that either a 5 MΩ/□ or a 20 MΩ/□ sheet resistivity provides cells with the proper resistance values. Cells are included that have all internal nodes accessible so that cells can also be tested without on chip cermet resistors utilizing off chip external resistors. For the design with the middle sized (2 μm, 4 μm wide) FETs, which are most likely sizes to be used, a version was layed out with substantially tighter design rules. Between RAM A and RAM B, the cells with external resistor connections of each size appear twice. All other variations appear either 4 or 5 times, and at least twice fully surrounded by neighboring cells. RAM C is a 2 × 2 array of RAM cells with 8 and 15 μm FETs, to be used for comparison with more well characterized device sizes. Also included are the cells with the tightened design rules, where each node of the circuit is accessible, to be used for failure analysis. These cell arrays will provide an extensive analysis of the design trade off considerations leading to a final, optimum RAM design.

The areas designated RAM 5, RAM 8, and RAM 7 are arrays of all the same cell; RAM 5 and RAM 8 are of the middle two FET sizes, with tightened

<table>
<tr><td>T2</td><td rowspan="2">FAT
FET
(CV)</td><td rowspan="2">FULL ADDER
WITH CORNER
GATE (ARG-PCM)</td><td rowspan="2">RAM
ARRAY
WITH
DAMAGED
RESISTORS</td><td>CURRENT
LIMITERS
1 μ & 2 μ</td><td>CERMET RES
1.0 μ,
DAMAGED R TEST</td></tr>
<tr><td>T1</td><td>CURRENT
LIMITERS
3 μ & 4 μ</td><td>CERMET RES
1.5 μ</td></tr>
<tr><td rowspan="2">FAT
FLT
(CV)
MOM</td><td>ELECT. ALIGN.
TEST (ARG-PCM-16A)</td><td colspan="2" rowspan="2">ANALOG GAIN TEST</td><td>CURRENT
LIMITERS
5 μ & 3/4 μ</td><td>CERMET RES
2.0 μ</td></tr>
<tr><td>DYN. RAM
TEST CELL</td><td>FETS
1 μ, 3 μ, 0.75 μ</td><td>DIODE LKGE
TESTS</td></tr>
<tr><td colspan="2">RAM A
RAM CELL VARIETY
WITH SMALLER FETS</td><td colspan="2">RAM B
RAM CELL VARIETY
WITH MEDIUM FETS</td><td colspan="2">RAM C
RAM CELLS
WITH LARGE FETS;
ALSO TIGHT RULES
VERIFICATION CELLS</td></tr>
<tr><td colspan="2">RAM 5
RAM CELL ARRAY
WITH SMALLER FETS,
TIGHT RULES</td><td colspan="2">RAM 8
RAM CELL ARRAY
WITH MEDIUM FETS,
TIGHT RULES</td><td colspan="2">RAM 7
RAM CELL ARRAY
WITH MEDIUM FETS,
NORMAL RULES</td></tr>
</table>

Fig. 3.2-1 Lot assignment map for AOSP RAM cell evaluation mask.

design rules, and RAM 7 is with normal design rules. The purpose of these arrays (containing 32 identical cells) is to provide yield data.

Other test structures include the self biasing current limiter in various sizes, several extremely small FETs, resistor test structures and diode leakage test patterns. A few other routine tests complete the mask.

This mask set was designed and digitized during this reporting period. Masks will be available by the first week of August. A fast process turn around is planned so that fabrication cells will be available for testing and evaluation in September. Results of this RAM cell concept study will allow the design of a 256 bit RAM in an effective and timely manner. Results on 256 RAM will be available during the fourth quarter of this program.

3.3 4K RAM Chip Organization

The development of a 4K bit RAM will require several design and process technology verification steps. These steps will range from the initial RAM cell study underway to a 256 RAM yield evaluation in the fourth quarter of this program and finally to the 4K RAM. In parallel with the technology development it is also important to conceptually design and understand how a 4K bit RAM chip will be developed using GaAs technology. The 4K bit RAM chip will consist of a 64 x 64 array of RAM cells, with every other row of cells inverted so adjacent rows can share + V_{DDA} and -V_{SSA} power buses, with row and column address decoders on the left and bottom respectively. The over all organization of the 4K power concentration RAM chip is shown in Fig. 3.3-1.

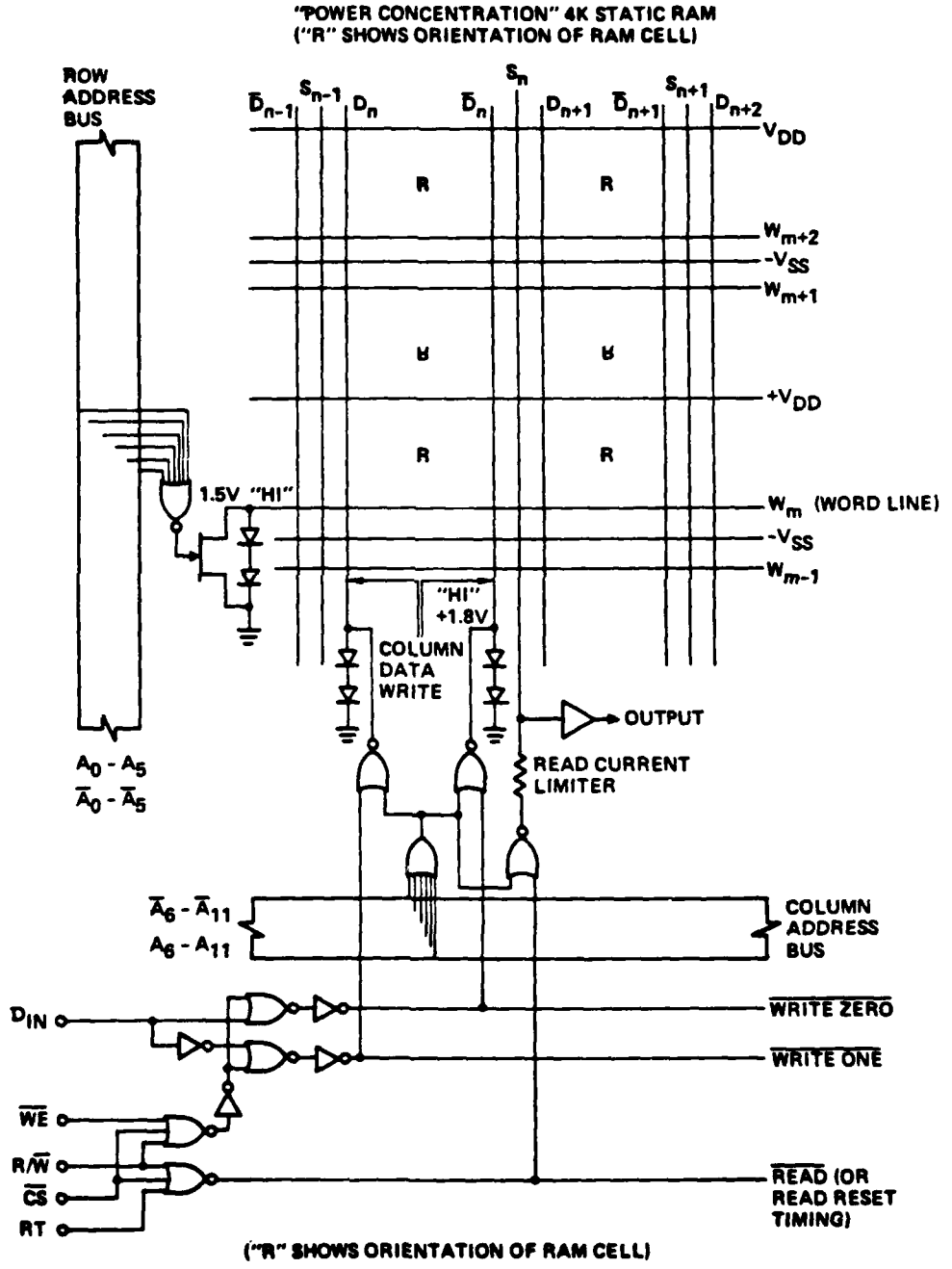


Fig. 3.3-1 Overall organization of power concentration RAM circuit showing row and column decoders, data write circuits and data read circuits.

Row and column decoders will consist of SDFL 1:64 demultiplexers which decode a 6 bit address to enable a row and column for read or write selection of one memory cell. The row decoders control the word line, enabling the row of memory cells when the selected word line is low. The column decoders control the data lines (D and $\overline{D}$) to write into the selected cell or the sense line (S) for nondestructively reading the contents of the selected cell.

The row and column address/write/ sense peripherals amount to the equivalent of about 400 logic gates. If all of these gates were left "on" all of the time, then even with the low power levels of SDFL, the static chip dissipation would be several hundred milliwatts from these peripherals alone, a hundred times higher than the AOSP static power budget for the whole chip. This makes it necesary to design into these peripherals automatic powerdown of portions of the peripheral circuitry not actually being used in a given access, and powerdown of all chip peripherals when the chip is not being accessed (chip enable, CE, "low"). By this means, the average power going to the peripheral circuitry will be much lower than the array static power in the AOSP application.

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